VOLTAGE CONTROLLED CRYSTAL OSCILLATORS
HCMOS 5V

FULL SIZE D.I.L.
M package
M2010, M2011
M2015, M2016

Phase-Locked Oscillator
Commercial: 0º to 70ºC
10 MHz to 44.736 MHz

FEATURES
- Cost-effective PLL solution which includes a VCXO, filter and phase detector in a single component
- Simplicity of design – requires only dividers to complete the loop
- Output frequency may be chosen at convenient frequency to create edges for desired timing waveforms
- Start up time less than 10 ms
- Guaranteed start-up with ramping DC Supply
- Inputs are TTL/HCMOS compatible

APPLICATIONS
- Regenerating and cleaning up noisy signals
- Low-jitter frequency multiplication

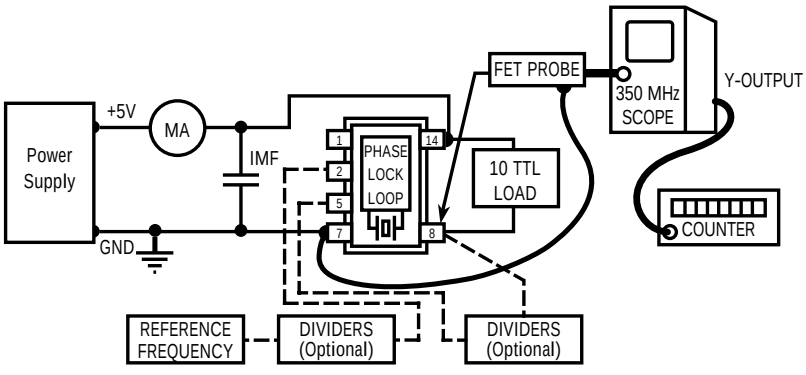
SPECIAL APPLICATION NOTE
Both the reference frequency and the output frequency, or submultiple, are input to the device. The two similar frequencies are compared, and an error signal is obtained which is applied to the VCXO. The VCXO frequency is then corrected and "locked" to the average value of the reference frequency.

The output frequency, usually chosen at a convenient frequency higher than the reference frequency, may then be used to generate desired timing waveforms.

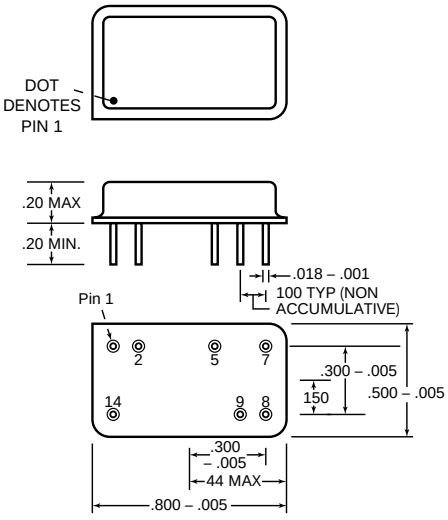
Description
These PLL sub-systems incorporate all the components required for phase locked loop functionality except the external frequency divider. The phase locked loop unit includes VCXO, phase comparator, and control voltage filter. It will lock the locally generated VCXO output to an incoming reference signal of the same or digitally-related frequency. An external divider between VCXO output and phase-detector input establishes the output/reference frequency ratio. Offered in a 5V DIL (M) package, the PLL modules are built around a VCXO with customer's choice of reference and output frequencies.

CONNECTIONS

	M2010 & M2015	M2011 & M2016
Pin 1.	Not used	Not used
Pin 2.	Frequency Input #1	Frequency Input #1
Pin 5.	Frequency Input #2	Frequency Input #2
Pin 7.	Ground	Ground and case
Pin 8.	Output Frequency	Output Frequency
Pin 9.	+5V	+5V
Pin 14.	+5V	+5V
All other pins are not present		



TEST CIRCUIT



"M-1" Package

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ELECTRICAL SPECIFICATIONS

Frequency Range 10 MHz to 44.736 MHz

Frequency Stability Includes calibration at 25°C, operating temperature, change of input voltage, change of load, shock and vibration.

	MIN	TYP	MAX	UNITS
Input Voltage	4.5	5.0	5.50	volts
Input Current (max. @ 5.5 VDC)		42	50	mA
Output Levels				
"0" Level, sinking 16 mA		0.4	0.5	volts
"1" Level, sourcing 8 mA	V_{DD}-.4			volts
Rise and Fall Times from 0.8 to 2.4V, 10 TTL		2.5	4	ns
Symmetry 10 TTL, @ 1.4V		45/55	40/60	percent
Aging				
First year		3		ppm
After first year		1		ppm/yr
Input Requirements for Pins 2 and 5				
Input Frequency, square wave				
Sinking at 0.4V		0.6	1.6	mA
Sourcing at 2.4V		100	400	mA

Reference Frequency Stability Requirements	
M2010, M2011	±125 ppm
M2015, M2016	±150 ppm

ENVIRONMENTAL SPECIFICATIONS

Temperature
Operating 0º to 70°C
Storage -55º to +125°C

Temperature Cycle – Not to exceed ±5 ppm change when exposed to 2 hours maximum at each temperature from 0 to 120°C, with 25°C reference

Shock – 1000 Gs, 0.35 ms, 1/2 sine wave, 3 shocks in each plane

Vibration – 10-2000 Hz of .06" d.a. or 20 Gs, whichever is less

Humidity – Resistant to 85° R.H. at 85°C

MECHANICAL SPECIFICATIONS

Gross Leak – Each unit checked in 125°C fluorocarbon

Fine Leak – Mass spectrometer leak rate less than 2 X 10^{-8} atmos, cc/sec of helium

Pins – Kovar, 7 microinch gold over nickel

Bend Test – Will withstand two bends of 90° from reference

Header – Steel, 7 microinch gold over nickel

Case – Stainless steel, type 304

Marking – Permanent black epoxy ink or laser marked

Resistance to Solvents – MIL STD 202, Method 215

HOW TO ORDER

M 2010-XXX.YYY

M is full size DIL	2010 is model type	Reference frequency code*	Output frequency code*	Leave blank for straight leads Add G for gullwing

*Consult factory for frequency codes.

SS#	Rev.
M2010	B

MF ELECTRONICS

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